

REMARKS

Claims 1-3, 5, 7-16, and 18-30 are now pending in the present application. By the present response, claims 4, 6, and 17 are canceled; claims 1, 5, 13-14, 16, and 24 are amended; and claims 28-30 are added. Reconsideration of the claims is respectfully requested.

The Examiner is thanked for indicating claim 27 to be allowable and for indicating other dependent claims to be allowable if made independent.

Applicants have submitted a proposed correction to the drawing labeled Figure 3 in red ink. This change corrects an error that was not discovered until after the application was filed and is supported by the specification on page 12, lines 13-17. The change will be incorporated into a formal set of drawings upon approval of the proposed change by the Examiner.

I. 35 U.S.C. § 102, Anticipation: Claims 1, 4-5, 8, 12, 14, 16, 19, and 23

Claims 1, 4-5, 8, 12, 14, 16, 19, and 23 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Ying et al., Fault Isolation and Recovery in a Distributed Control Network, U.S. Patent No. 6,147,967, November 14, 2000 (hereinafter “Ying”). This rejection is respectfully traversed.

In order to take the most easily allowable claims, claims 1 and 14 have been amended to incorporate the allowable subject matter of claims 6 and 17 respectively. Since claims 4-5, 8, 12, 16, 19, and 23 depend from either claim 1 or claim 14, the same distinctions between Ying and the claimed invention in claims 1 and 14 are now present in these claims also. Consequently, it is respectfully urged that the rejection of claims 1, 4-5, 8, 12, 14, 16, 19, and 23 are moot.

II. 35 U.S.C. § 103, Obviousness: Claims 2, 3, 13, 15, and 24

Claims 2, 3, and 15 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Barenys et al., Method for Isolating an I2C Bus Fault Using Self Bus Switching Device, U.S. Patent Publication No. 2002/0108076, August 8, 2002 (hereinafter “Barenys”). This rejection is respectfully traversed.

Additionally, claims 13 and 24 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Bandholz et al., Apparatus for Supporting I2C Bus Masters on a Secondary

Side of an I2C Multiplexor, U.S. Patent Publication No. 2003/0212847, November 13, 2003
(hereinafter “**Bandholz**”). This rejection is respectfully traversed.

Each of the claims in these two rejections is dependent on either claim 1 or claim 14, both of which have been amended to contain allowable matter. Therefore, the 103 rejections above are now moot.

III. Objection to Claims: Claims 6, 7, 9-11, 17, 18, 20-22, 25, and 26

The examiner has stated on pages 7-8 of the Office Action dated September 26, 2005 that claims 6, 7, 9-11, 17, 18, 20-22, 25, and 26 were objected to for being dependent on a rejected claim. However, as noted above, the subject matter of claim 6 has now been incorporated into claim 1 and the subject matter of claim 17 has been incorporated into claim 14. All claims are now allowable.

IV. New Claims

Newly added dependent claims 28-30 are added to recite additional features not previously recited in the claims. Claim 28 now recites “said address stored in said address logic overriding all of the bits of said hardwired address”, while claim 30 recites a method claim version of this feature. This feature is supported by the application on page 12, line 27 through page 13, line 8. Claim 29 recites the results of an additional switch setting in which the I²C device is not itself logically connected to the I²C bus, but will pass the bus signal downstream.

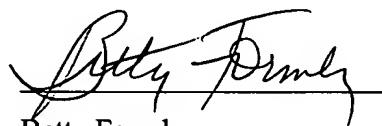
V. Conclusion

It is respectfully urged that the subject application is patentable over the cited references and is now in condition for allowance.

The examiner is invited to call the undersigned at the below-listed telephone number if in the opinion of the examiner such a telephone conference would expedite or aid the prosecution and examination of this application.

DATE: December 22, 2005

Respectfully submitted,



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IN THE DRAWINGS:

A proposed amendment to Figure 3 is shown in red on that figure. The amendment adds a connection from I2C device 300 to pin 332.